NEC

PRODUCT DESCRIPTION
µPD7764

NEC ELECTRONICS (EUROPE) GMBH

PRODUCT DESCRIPTION

µPD7764

3/85 V1.0

VOICE RECOGNITION PROCESSOR

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FOREWORD

The μPD7764D is a microprocessor suited for voice recognition processing. It is provided with two independent processors; one calculates the distance between the voice data (i.e., patterns) and the other controls the μPD7764D. These enable high-speed execution of voice pattern matching operations such as DP matching. Moreover, since RAMs are employed for program memory, various matching algorithms can be used.

CHAPTER 1 OUTLINE

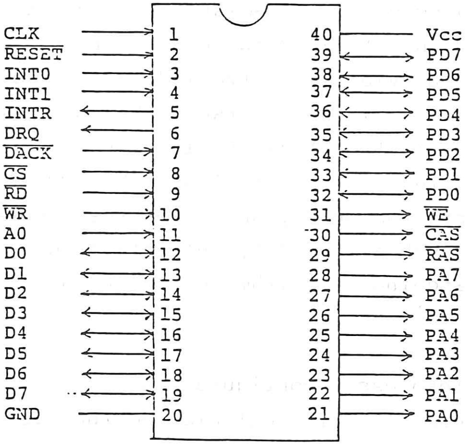
In a voice recognition system, matching between an input non-registered voice and a registered voice is frequently performed. The μPD7764D is an LSI for this purpose. It is internally provided with two independent processors; one calculates the distance between the voice patterns and the other controls the μPD7764D. These processors realize high-speed matching operations. Since the μPD7764D incorporates RAMs for program memory and a ROM that contains the basic utilities such as the IPL, multiplication, division, etc., various matching algorithms can be used.

1.1 Features

- ° Multiprocessor configuration
  - D processor for calculating the distance between the voice patterns
  - G processor for controlling and matching operations
- ° Memory capacity
  - D processor
    - . Instruction RAM : 32 x 16 bits
    - . Pattern buffer RAM : 416 x 8 bits
  - G processor
    - . Instruction RAM : 128 x 16 bits
    - . Data RAM: : 88 x 16 bits
- ° Basic utility routines incorporated
- ° Instruction cycle : 250ns (Clock frequency: 8MHz)
- ° Subroutine levels : 8
- ° Bus interface : With 80-family CPU
- ° DMA interface incorporated
- ° Reference data (DRAM) management function provided
- ° Two levels of external interrupt inputs
- ° Process : NMOS
- ° Power source : 5V single power source
- ° Package : 40-pin ceramic DIP

CHAPTER 2 PIN FUNCTIONS

2.1 Pin Configuration (Top View)



2.2 Pin Functions

(1) CLK (clock) Input

This pin inputs a single-phase clock with a frequency of 8MHz.

(2) $\overline{\text{RESET}}$ (reset) Input

This pin inputs the reset signal for system initialization.

The reset signal must be held low for a duration of at least four clocks.

(3) INT0 and INT1 (interrupts) Input

These pins input interrupt requests. The INT0 signal takes precedence over the INT1 signal.

(4) INTR (interrupt request) Output

This pin outputs an interrupt request.

(5) DRQ (DMA request) Output

This pin outputs the DMA request signal.

(6) $\overline{\text{DACK}}$ (DMA acknowledge) Input

This pin inputs an acknowledge signal the host processor sends in response to µPD7764D's DMA requests.

(7) $\overline{\text{CS}}$ (chip select) Input

This pin inputs the chip select signal. When a low-level signal is input to this pin, the input/output of the data bus is enabled.

(8) $\overline{\text{RD}}$ (read strobe) Input

A low-level strobe signal is input to this pin when the host processor is to read data from the μPD7764D.

(9) $\overline{\text{WR}}$ (write strobe) Input

A low-level strobe signal is input to this pin when the host processor is to write data to the μPD7764D.

(10) A0 (address bus) Input

This pin selects the register (SR or DR) that inputs/outputs data via the data bus pins.

(11) D0 to D7 (data bus) Input/Output (three-state)

These eight pins function as a bidirectional 8-bit data bus.

(12) GND (ground)

This is a ground pin.

(13) PA0 to PA7 (pattern memory address bus) Output

These output an address signal to the external pattern memory.

(14) $\overline{\text{RAS}}$ (row address strobe) Output

This pin outputs a control signal that indicates that the signals output to pins PA0 through PA7 are a row address.

(15) $\overline{\text{CAS}}$ (column address strobe) Output

This pin outputs a control signal that indicates that the signals output to pins PA0 through PA7 are a column address.

(16) $\overline{\text{WE}}$ (write enable) Output

This pin outputs a control signal that enables data output to pins PD0 through PD7 to be written to the external pattern memory.

(17) PD0 to PD7 (memory data bus) Input/Output (three-state)

These pins function as a bidirectional 8-bit data bus used to transfer data between the external pattern memory and the μPD7764D.

(18) V_{CC} (+5V power supply)

This is a power pin (+5V).

CHAPTER 3 INTERNAL FUNCTIONS

The μPD7764D can be functionally divided into three independent parts: G-PART, D-PART, and IO-PART. The functions of each part are as follows when the μPD7764D performs processing.

° G-PART :	Performs calculation of the recurrence formula in the DP matching based on the distance between the voice patterns.
° D-PART :	Determines the distance between the voice patterns from the reference data and input voice data.
° IO-PART:	Controls the external pattern memory and input/output operation of the μPD7764D.

The block diagram of the μPD7764D is shown in Fig. 3-1.

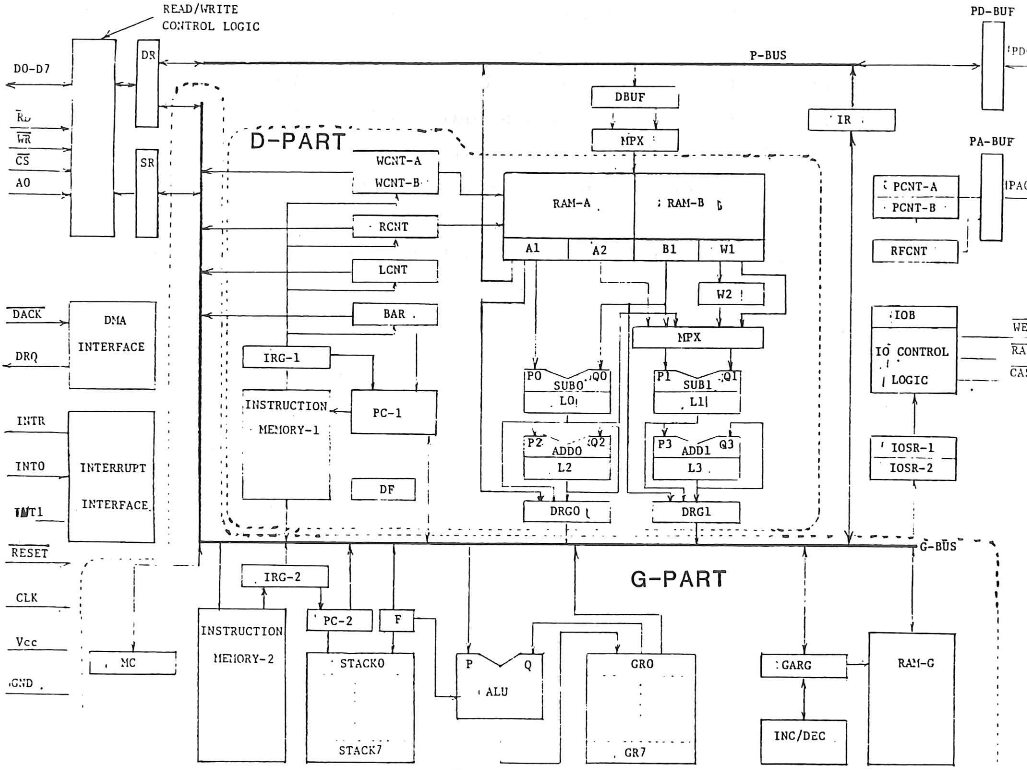


Fig. 3-1 Block Diagram of μPD7764D

3.1 Functions of G-PART

(1) IRG2 (instruction register)

This is a 16-bit instruction register of G-PART.

(2) Instruction memory 2

This is a memory in which the program of G-PART is stored. It has a capacity of 256 words (16 bits per word). The first 128 words of the memory are used as a RAM, in which programs can be exchanged. The remaining 128 words are used as a ROM that stores the basic utilities. The addresses of instruction memory 2 are specified by program counter PC2.

(3) PC2 (program counter 2)

This is an 8-bit binary counter that specifies the addresses of instruction memory 2. Normally, the PC2 is incremented to indicate the next address each time an instruction is fetched. In accordance with the operation of the PC2, the instructions are successively read from instruction memory 2. When a jump or subroutine call instruction is executed, the contents of the address field of the instruction are transferred to the PC2. When a return instruction is executed, the contents of the stack register are transferred to the PC2.

(4) MC (memory counter)

The MC is a 10-bit counter that consists of two independent counters. The lower 7 bits are used as a binary counter that specifies the address of instruction memory 2 when data is to be written to the memory. This counter is incremented each time data is written. The higher 3 bits are used as the counter of modulo 6 which is used to specify the device that outputs data to the GBUS.

(5) Stack

This is a group of registers that store return addresses and flags when a subroutine call instruction is executed or when an interrupt is generated.

The stack consists of eight registers, each of which has 13 (9+4) bits, for an eight-level LIFO (last-in, first-out) configuration. When the return instruction is executed, the return address (i.e., the contents of the higher 9 bits of each register) is transferred to the PC2, whereas the flags (the contents of the lower 4 bits of the register) are transferred to the F register.

(6) RAMG

This is a RAM which stores data and has a configuration of 4 banks x 22 words x 16 bits. The addresses of RAMG are specified by the GARG register. Data in RAMG can be read in byte units as well as in word units.

(7) GARG

This is a 10-bit register that contains an address of data in RAMG. The GARG consists of three fields, each of which specifies:

° A bank

° An address in a bank

° Units being used to access RAMG

GARG Configuration and Addressing

(1) Bit configuration of GARG

D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ACCE		H	SL	L	Index				

Note: The index field contains an address in the selected bank.

(2) Bank

H	SL	L	Bank No.
-	0	0	0
-	0	1	1
0	1	-	2
1	1	-	3

(3) Unit

ACCE	Accessing unit
0 0	Word (16 bits)
0 1	Higher 8 bits
1 0	Lower 8 bits
1 1	(Disabled)

(8) INC/DEC (increment/decrement)

The INC/DEC modifies the contents of data memory address register GARG. It increments/decrements the index field of GARG with modulo 22, and sets/resets each bit of the ACCE, H, SL, and L fields.

(9) ALU

This is a 16-bit arithmetic and logical unit that performs arithmetic operations such as addition, bit inversion, logical OR, logical AND, and exclusive OR. It also performs shift operation. The Q input and the output of the ALU are applied from/to one of general-purpose registers GR0 through GR7 and the P input is applied by the GBUS.

(10) GR0 - 7 (general registers)

These eight registers are 16-bit general-purpose registers.

(11) F (Flag)

This is a flag register that consists of the Z (zero), C (carry), S (sign), and OV (overflow) flags. The contents of this register are updated according to the result of ALU operations.

3.2 Functions of D-PART

(1) IRG1 (instruction register)

This is a 16-bit instruction register of D-PART.

(2) Instruction memory 1

This is a RAM that stores the program of D-PART and its configuration is 16 bits x 32 words.

(3) PC1 (program counter 1)

This is a 6-bit binary counter that specifies the address of instruction memory 1. The most significant bit (MSB) of the PC1 specifies whether write or read operation is performed on instruction memory 1.

(a) When the MSB of PC1 is "0"

The PC1 is incremented each time an instruction is fetched and instructions are successively read from instruction memory 1.

(b) When the MSB of PC1 is "1"

The PC1 increments each time the GBUS writes an instruction to instruction memory 1.

(4) LCNT (loop counter)

This is a decremental counter that counts the repetitive processes performed by the D-PART. The higher 8 bits and lower 8 bits respectively serve as independent counters $LCNT_H$ and $LCNT_L$.

(5) BAR (branch address register)

The BAR consists of two branch address registers. The higher 6 bits of the BAR are used as address register BAR_H, while the lower 6 bits serve as address register BAR_L.

If the contents of the $LCNT_H$ or $LCNT_L$ are not 0 as a result of decrementing the loop counter, the contents of the corresponding BAR (BAR_H or BAR_L) are transferred to the PC1.

(6) RCNT

This is a 9-bit up counter that specifies the address of RAMA or RAMB when the data are to be read from the RAMs to buffer A_1, A_2, B_1, or W_1. The lower 4 bits specify the address in a banks of RAMA or RAMB. The higher 5 bits serve as a counter with modulo 22 and specify the bank of RAMA only. When the data is to be read from RAMB, the bank must be specified by the bank-specifying field of the WCNTB.

Specifying RAMA Bank to be Read

<table>
<tr><th></th><th>D8</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>RCNT</td><td colspan="5">Specifies RAMA bank for data read</td><td colspan="4">Specifies address in RAMA/RAMB bank</td></tr>
</table>

RAMA bank specifying field	Bank to be read	
	A1	A2
B	B	B+1

$0 \le B \le 21$

(7) WCNTA and WCNTB

These are counters that contain the address of RAMA or RAMB to which data held in data buffer DBUF are to be written. The WCNTA is a 9-bit counter. The higher 5 bits of this counter (modulo 22) specify the bank of the RAM independent of the lower 4 bits. Similarly, the higher 2 bits of the WCNTB (modulo 4), which is a 6-bit counter, are independent of the lower 4 bits. The bank-specifying field of the WCNTB is referred when data are read from RAMB.

Specifying RAMB Bank to be Read

	D8 D7 D6 D5 D4	D3 D2 D1 D0
WCNTA	Specifies RAMA bank for data write	Specifies address in RAMA bank

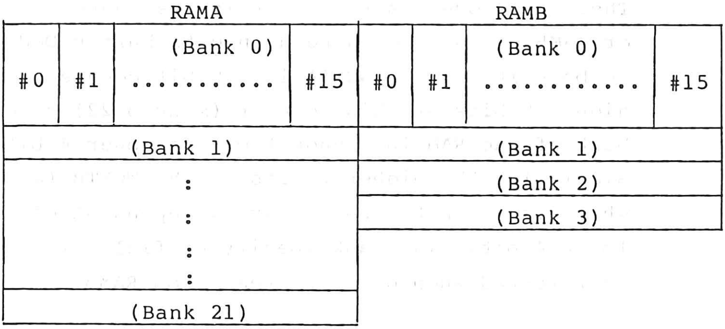
	D5 D4	D3 D2 D1 D0
WCNTB	Spec-ifies RAMB bank	Specifies address in RAMB bank

WCNTB bank specifying field	Bank read to output buffer	
	B1	W1
0 or 1	2	3
2 or 3	0	1

(8) RAMA and RAMB

RAMA is configurated as 1 byte x 16 words x 22 banks, while RAMB is configured as 1 byte x 16 words x 4 banks.

Configuration of RAMA and RAMB



Note: ° Each bank has the same configuration as bank 0.
° The word length of #n is 8 bits. ($0 \leq n \leq 15$)

Specifying RAMA and RAMB Addresses

Operation	Address specifying register	
	Bank is specified by:	Address in bank is specified by:
Write to RAMA	$WCNTA_H$	$WCNTA_L$
Read from RAMA	$RCNT_H$	$RCNT_L$
Write to RAMB	$WCNTB_H$	$WCNTB_L$
Read from RAMB	$WCNTB_H$*	$RCNT_L$

* Refer to the table titled "Specifying RAMB Bank to be Read".

Note: The suffix H denotes the bank-specifying field, which consists of the higher register bits. Suffix L denotes the bank address-specifying field consisting of the lower register bits.

(9) SUB0 and SUB1 (subtracters 0 and 1)

These are 8-bit subtracters that perform one of these arithmetic operations.

(a) Subtraction only

(b) Obtaining the absolute value after subtraction

(c) Replacing the result of the subtraction with zero (0) if it is negative

The SUB0 and SUB1 are provided with output latches L0 and L1, respectively.

(10) ADD0 and ADD1 (adders 0 and 1)

These are 12-bit adders. The L2 is the output latch of the ADD0, while the L3 is of the ADD1.

(11) DRG0 and DRG1 (data registers 0 and 1)

These are 16-bit registers that store the results of processing performed in D-PART. They also function as an interface when data are transferred to G-PART.

(12) DF (D-PART flag)

This is a 1-bit flag which functions as an interface when the D-PART is controlled along with G-PART. G-PART can reset this flag using an instruction. The flag can be set or reset by an instruction from D-PART. The contents of the DF flag can be specified as a condition of the branch instruction for G-PART.

3.3 Functions of IO-PART

(1) SR (status register)

This is an 8-bit register that holds information concerning interfacing with the host processor.

Configuration of SR Register

D7	D6	D5	D4	D3	D2	D1	D0
USF	EI1	EI0	DMA	DRC	DRS	RQM	

(a) USF (user flag)

This flag can be defined by user.

(b) EI0 and EI1 (enable interrupt)

The EI0 and EI1 are flags that indicate whether interrupts to be initiated by the INT0 and INT1 signals are enabled or disabled.

(c) DMA (direct memory access)

To transfer data between an external system and the DR register via pins D0 through D7, two methods are available. One is through handshaking (non-DMA) by which the contents of the SR register are checked during data transfer. The other method is DMA transfer accomplished using the DRQ and $\overline{\text{DACK}}$ signals. This DMA bit is used to determine which of the two methods is to be employed.

"0": Non-DMA method
"1": DMA method

(d) DRC (DR control)

This is the bit used to select the bit configuration of the DR register.

"0": DR register serves as a 16-bit register.
"1": DR register serves as an 8-bit register.

(e) DRS (DR status)

This bit indicates the data transfer status when the DR register is used as a 16-bit register.

"1": Only the first 8 bits of the data have been transferred.
"0": The last 8 bits of the data have also been transferred.

(f) RQM (request for master)

The RQM comprises flag bits that indicate the status of the data transfer between the DR register and the host processor.

00 : Indicates that the external host processor has read/written data from/to the DR register.

01*: Indicates that the data on the internal data bus (PBUS or GBUS) are written to the DR register (output request).

10*: Indicates that the data stored in the DR register are read to the internal data bus (input request).

* Some instructions do not cause these bits to be set.

(2) DR

The DR is a 16-bit register that transfers data to/from the external device via the data bus consisting of pins D0 to D7. Pins D0 to D7 are used to transfer 8-bit data. Since the data bus comprises 8 bits, when 16-bit data is to be transferred, is divided into two and 8 bits are transferred at a time. When this register is defined as an 8-bit register by the DRC bit of the SR register, the lower 8 bits of the DR register are transferred.

(3) Read/write control logic

This logic controls data transfer to/from the external device via pins D0 through D7.

Read/Write Control Logic Operation

$\overline{CS}$	A0	$\overline{WR}$	$\overline{RD}$	Operation
1	-	-	-	Internal operations does not affected.
-	-	1	1	Pins D0 through D7 are high-impedance.
0	0	0	1	Data on pins D0 through D7 are latched to DR register.*
0	0	1	0	Contents of DR register are output to pins D0 through D7*.
0	1	0	1	Inhibited
0	1	1	0	Contents of SR register are output to pins D0 through D7.
0	-	0	0	Inhibited

* Either the higher or lower 8 bits of the DR register can be selected by the DRS bit of the SR register.

(4) IOSR1 and IOSR2

These are 16-bit registers that hold control data of the I/O control logic. Neither input nor output of data affects the contents of these registers.

Bit Configuration of IOSR1/2

D	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	COUNT								PBUS SRC		PBUS DST		RC	SL	WS	

(a) COUNT

These bits indicate the number of times the data are to be transferred via the PBUS.

(b) PBUS SRC (PBUS source)

These bits specify the register whose data are to be output to the PBUS. When the PDBUF is specified, data are read from the external device via pins PD_0 through PD_7.

(c) PBUS DST (PBUS destination)

These bits specify the register to which data are input from the PBUS. When the PDBUF is specified, data input to the PDBUF are written to the external memory via pins PD_0 through PD_7.

(d) RC

When the DR or IR register is specified by the PBUS SRC or PBUS DST, this bit specifies the data transfer method to be used (i.e., when this bit is 1, 16-bit data is transferred, and when it is 0, 8-bit data is transferred).

(e) SL

When the PDBUF is specified by the PBUS SRC, this bit specifies address register PCNTA or PCNTB. When the PDBUF is specified by the PBUS DST, this bit specifies RAMA or RAMB.

(f) WS

When the DBUF is specified by the PBUS DST, these bits specify the operation of the DBUF.

(5) IOB

This is a flag that indicates whether data input performed by the I/O control logic is in progress or complete.

(6) I/O control logic

This part controls the PBUS and data transfer via pins PD_0 through PD_7 and is also provided with a function to refresh the external memory.

When the IOB flag is set to 1, the I/O control logic loads the I/O control information of the IOSR1 and inputs/outputs the quantity of data specified. It then performs the loading of the I/O control information and inputting/outputting data for the IOSR2 in the same manner as for the IOSR1. It then clears the IOB flag to 0.

(7) PCNTA and PCNTB

These are 16-bit binary counters used to specify the address when data transfer is performed to/from the external memory via pins PD_0 through PD_7. These counters are incremented each time data is input or output through the PDBUF.

(8) RFCNT (refresh counter)

This is an 8-bit counter used to refresh the external memory connected to pins PD_0 through PD_7.

(9) DBUF

This is a buffer that holds data output to the PBUS which is to be written to RAMA or RAMB. Either 4-bit or 8-bit data can be retained by this buffer for data write.

(10) IR

This is a 16-bit register used when the GBUS inputs/outputs data to/from the external device via pins PD_0 through PD_7. The IOB flag is set when data is transferred between the IR register and GBUS.

(11) DMA interface

This interface controls the DRQ signal by using the $\overline{\text{DACK}}$ signal. The DRQ signal is a DMA request signal that requests the host processor or DMA controller to perform DMA transfer.

(12) Interrupt interface

This circuit specifies an interrupt address and controls the interrupt when it is generated by the INT0 or INT1 signal.

(13) RESET

This signal initializes the system. To do so, it must be input for a duration of at least four clocks. The flags and registers are initialized as follows:

Registers Affected by RESET Signal and Their Value

Functional classification	Name	Initial value
Program Counter	PC1 PC2 MC	20H 80H 0
Flag	F (C, Z, OV, S) DF IOB	0 0 0
Register	SR	0
Refresh Counter	RFCNT	FFH

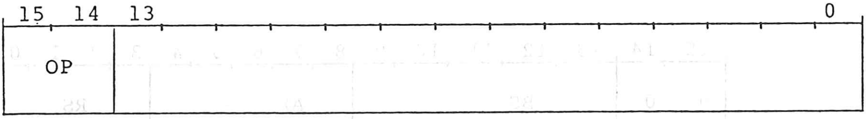
CHAPTER 4 INSTRUCTIONS

G-PART and D-PART of the μPD7764D each have respective instruction memories and instruction sets, each of which is independent of the other, whereas IO-PART regards control information written to the IOSR1 or IOSR2 register as an instruction.

4.1 G-INSTRUCTION

Instructions for G-PART (hereinafter referred to as "G-INSTRUCTION") are classified into the four types listed in the table below. This classification is made in accordance with the OP field of a 16-bit instruction, which is the highest 2 bits of the instruction.

Configuration of G-INSTRUCTION and OP Field Position



Classification of G-INSTRUCTION by OP Code

OP		Instruction	Word	Machine cycle	Operation
D15	D14				
0	0	OP instrution	1	1	ALU operation
0	1	LD instruction	2	2	1st cycle: ALU operation 2nd cycle: Loading immediate data
1	0	MV instruction	1	1	transfer
1	1	JP instruction	1	1	Jump (Conditional/unconditional, Jump/ subroutine call)

Moreover, the instruction code of each instruction is divided into two or three fields as shown below.

Four Types of G-INSTRUCTIONs and Their Bit Configuration

Instruction	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OP	0	0	BS					ALU					RS			
LD	0	1	BS					ALU					RS			
MV	1	0	SRC					DST					GM			
JP	1	1	T	CND				NA*								

* Next address

(1) OP instruction

The OP instruction consists of an OP code and three fields as illustrated below.

OP Instruction Configuration

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	BS					ALU					RS			

The OP instruction has the following functions.

- It performs the operation specified by the above three fields.
- It increments the PC2.

Each field functions as follows:

(a) BS field

This field specifies the register whose contents are to be input to the ALU as its P input and modifies the GARG.

When modified, the value of the GARG register becomes valid from the next instruction.

(b) ALU field

This field consists of 5 bits and specifies the function of the ALU. The highest bit of the ALU field (D8) is 0 when there is only one operand. The D8 bit is 1 when the number of the operands is two.

(c) RS field

This field specifies one of general-purpose registers GR0 to GR7, which can be either Q-input to ALU OR output.

(2) LD instruction

The bit configuration of the LD instruction is as illustrated below. The BS, ALU, and RS fields of this instruction have the same functions as those of the OP instruction.

Field Configuration of LD Instruction

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
OP		BS					ALU					RS				1st word

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
ID																2nd word

The LD instruction performs the following operations.

° In the first machine cycle, perform the ALU operation and increments the PC2.

° In the second machine cyle, the immediate data (ID) fetched from instruction memory 2 is transferred to the register specified by the BS field via the internal bus.
If an instruction in the BS field specifies the modification to the GARG, the immediate data are output to the modified address.

° Increments the PC2.

(3) MV instruction

The MV instruction consists of an OP code, DST (destination) field, SRC (source) field, and GM (GARG modify) field as illustrated below.

Field Configuration of MV Instruction

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">OP</td><td colspan="5">SRC</td><td colspan="5">DST</td><td colspan="4">GM</td></tr>
</table>

When the MV instruction is executed, data is transferred through the GBUS. The functions of this instruction are as follows:

(a) Outputs the contents of the register specified by the SRC field to the GBUS.

(b) Inputs the data output to the GBUS to the register specified by the DST field.

(c) Executes the GARG-modifying instruction specified by the GM, SRC, and DST fields.

(d) If both the SRC and DST fields contain a modifying instruction, only that specified by the SRC field is executed.

(e) The modified value of the GARG becomes valid from the next instruction for data read. However, it becomes valid from that instruction for data write.

(f) If the GARG register is specified by the DST field, the GARG-modifying instruction is invalid.

(g) Increments the PC2.

(4) JP instruction

Field Configuration of JP Instruction

15 14	13	12 11 10 9	8 7 6 5 4 3 2 1 0
OP	T	CND	NA

The JP instruction functionally consists of a branch condition, a jump or subroutine call instruction, and a return instruction.

(a) T field

This field is used to distinguish the jump instruction from the subroutine call instruction.

Functions Specified by T Field

T	Function	
D13	D9=0	D9=1
0	JUMP	Flags are not saved to the stack.
1	CALL	Data for flags are transferred from the stack.

(b) CND field (Condition)

This field provides the branch condition.

Note: The return instruction code is embedded in the CND field and then the T field specifies the F data transfer operation. The NA field in the return instruction code is ignored.

Conditions Specified by CND Field

CND field				Condition
D12	D11	D10	D9	
0	0	0	0	Unconditional
0	0	0	1	(Return instruction)
0	0	1	0	C=0
0	0	1	1	C=1
0	1	0	0	Z=0
0	1	0	1	Z=1
0	1	1	0	OV=0
0	1	1	1	OV=1
1	0	0	0	S=0
1	0	0	1	S=1
1	0	1	0	IOB=0
1	0	1	1	IOB=1
1	1	0	0	DF=0
1	1	0	1	DF=1
1	1	1	0	RQM=0
1	1	1	1	RQM≠0

(c) NA field (next address)

This field specifies the destination to which the program execution is to be branched by the jump or subroutine call instruction.

(5) List of G-INSTRUCTION operations

(a) Registers specified by the BS, DST, and SRC fields

Field / Instruction	OP instruction	LD instruction	MV instruction
BS 13 12 11 10 9	Specifies P input of ALU	Specifies P input of ALU. Destination of immediate data	———
DST 13 12 11 10 9	———	———	Destination
SRC 8 7 6 5 4	———	———	Destination
0 0 0 0 0	NON	No register is specified.	
0 0 0 0 1	SR	SR	
0 0 0 1 0	DR	DR	
0 0 0 1 1	DRNF	DR (RQM flag is not set.)	
0 0 1 0 0	IR	IR	
0 0 1 0 1	PC1	PC1	
0 0 1 1 0	IM1	Instruction memory 1	
0 0 1 1 1	IM2	Indirectly specifies MC_H.*	
0 1 0 0 0	GR0	GR0	
0 1 0 0 1	GR1	GR1	
0 1 0 1 0	GR2	GR2	
0 1 0 1 1	GR3	GR3	
0 1 1 0 0	GR4	GR4	
0 1 1 0 1	GR5	GR5	
0 1 1 1 0	GR6	GR6	
0 1 1 1 1	GR7	GR7	
1 0 0 0 0	GARG	GARG	
1 0 0 0 1	MC	MC	
1 0 0 1 0	DRG0	DRG0	
1 0 0 1 1	DRG1	DRG1	
1 0 1 0 0	IOSR1	IOSR1	
1 0 1 0 1	IOSR2	IOSR2	
1 0 1 1 0	PCNTA	PCNTA	
1 0 1 1 1	PCNTB	PCNTB	
1 1 0 0 0	M	RAMG**	
1 1 0 0 1	MCLR		
1 1 0 1 0	MINC		
1 1 0 1 1	MDEC		
1 1 1 0 0	MBC		
1 1 1 0 1	MBCLR		
1 1 1 1 0	MBCINC		
1 1 1 1 1	MBCDED		

*The higher 3 bits of the memory counter (MC). Refer to the table on the next page.

**Refer to the table (c).

(b) Registers selected when the MC_H is specified

<table>
<tr><td>MC_H</td><td colspan="16">Output to GBUS</td></tr>
<tr><td>9 8 7</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>0 0 0</td><td colspan="16">Instruction memory 2 (16 bits)</td></tr>
<tr><td rowspan="2">0 0 1</td><td rowspan="2">0</td><td rowspan="2">0</td><td rowspan="2">0</td><td colspan="4">F</td><td colspan="9" rowspan="2">PC2</td></tr>
<tr><td>S</td><td>OV</td><td>Z</td><td>C</td></tr>
<tr><td>0 1 0</td><td>0</td><td>0</td><td colspan="6">BAR_H</td><td>0</td><td>0</td><td colspan="6">BAR_L</td></tr>
<tr><td>0 1 1</td><td colspan="8">$LCNT_H$</td><td colspan="8">$LCNT_L$</td></tr>
<tr><td>1 0 0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="9">RCNT</td></tr>
<tr><td>1 0 1</td><td>0</td><td colspan="9">WCNTA</td><td colspan="6">WCNTB</td></tr>
</table>

(c) Functions specified by BS and SRC fields

BS, SRC, and DST fields	Functions for GARG	
	Mnemonic	Function
11000	M	No operation
11001	MCLR	(INDEX)←0
11010	MINC	(INDEX)←(INDEX)+1
11011	MDEC	(INDEX)←(INDEX)-1
11100	MBC	(L)←(L)
11101	MBCCLR	(L)←($\underline{L}$) (INDEX)←0
11110	MBCINC	(L)←($\underline{L}$) (INDEX)←(INDEX)+1
11111	MBCDEC	(L)←($\underline{L}$) (INDEX)←(INDEX)-1

INDEX: Lower 5 bits of the GARG (D4 to D0)
L : Bit D5 of the GARG

(d) ALU FUNCTIONS

ALU function I (Operation with one operand)

ALU field					Mnemonic	ALU function	
D8	D7	D6	D5	D4			
0	0	0	0	0	NOP	No operation	
0	0	0	0	1	CLR	Clear	$(R) \leftarrow 0$
0	0	0	1	0	INC	Increment	$(R) \leftarrow (R)+1$
0	0	0	1	1	DEC	Decrement	$(R) \leftarrow (R)-1$
0	0	1	0	0	CPL1	1's complement	$(R) \leftarrow \overline{(R)}$
0	0	1	0	1	CPL2	2's complement	$(R) \leftarrow \overline{(R)}+1$
0	0	1	1	0	SHRA	Arithmetic right shift	$(R)_n \leftarrow (R)_{n+1}$ $(C) \leftarrow (R)_0$, $(R)_{15} \leftarrow (R)_{15}$
0	0	1	1	1	SHLA	Arithmetic left shift	$(R)_n \leftarrow (R)_{n-1}$ $(R)_0 \leftarrow 0$, $(C) \leftarrow (R)_{15}$
0	1	0	0	0	SHR1	1-bit right shift	$(R)_n \leftarrow (R)_{n+1}$ $(R)_{15} \leftarrow (C)$, $(C) \leftarrow (R)_0$
0	1	0	0	1	SHL1	1-bit left shift	$(R)_n \leftarrow (R)_{n-1}$ $(C) \leftarrow (R)_{15}$, $(R)_{15} \leftarrow (C)$
0	1	0	1	0	SHR2	2-bit right shift	$(R)_n \leftarrow (R)_{n+2}$ $(R)_{15}$, $(R)_{14} \leftarrow 0$
0	1	0	1	1	SHL2	2-bit left shift	$(R)_n \leftarrow (R)_{n-2}$ $(R)_1 (R)_0 \leftarrow 0$
0	1	1	0	0	SHR4	4-bit right shift	$(R)_n \leftarrow (R)_{n+4}$ $(R)_{15}$, $(R)_{14}$, $(R)_{13}$, $(R)_{12} \leftarrow 0$
0	1	1	0	1	SHL4	4-bit left shift	$(R)_n \leftarrow (R)_{n-4}$ $(R)_3$, $(R)_2$, $(R)_1$, $(R)_0 \leftarrow 0$
0	1	1	1	0	SWAP		$(R)_n \rightleftarrows (R)_{n-8}$, $15 > n > 8$
0	1	1	1	1		Inhibited	

(R) : denotes one of the general-purpose registers GR0 to GR7 specified by the RS field.

$(R)_n$: denotes the nth bit of the (R).

(C) : denotes the carry flag.

ALU Function II (Operation with Two Operands)

ALU field					Mnemonic	ALU function	
D8	D7	D6	D5	D4			
1	0	0	0	0		Inhibited	
1	0	0	0	1	OR	OR	$(R) \leftarrow (R) \vee (B)$
1	0	0	1	0	AND	AND	$(R) \leftarrow (R) \wedge (B)$
1	0	0	1	1	XOR	Exclusive OR	$(R) \leftarrow (R) \vee (B)$
1	0	1	0	0	SUB	Subtract	$(R) \leftarrow (R) - (B)$
1	0	1	0	1	ADD	Add	$(R) \leftarrow (R) + (B)$
1	0	1	1	0	SBB	Subtract with borrow	$(R) \leftarrow (R) - (B) - (C)$
1	0	1	1	1	ADC	Add with carry	$(R) \leftarrow (R) + (B) + (C)$
1	1	0	0	0	MIN	Minor	$(R) \leftarrow (B)$ if $(B) - (R) < 0$
1	1	0	0	1	CMPR	Compare	$(R) - (B)$
1	1	0	1	0	SUBI	Subtract inversely	$(R) \leftarrow (B) - (R)$
1	1	0	1	1		Inhibited	
1	1	1	0	0	SUBP	Protected* subtract	* (SUB)
1	1	1	0	1	ADDP	Protected add	* (ADD)
1	1	1	1	0	SBBP	Protected* subtract with borrow	* (SBB)
1	1	1	1	1	ADCP	Protected add with carry	* (ADC)

(B) : denotes the register specified by the BS field.

*( ) : denotes the result of the operation indicated in parentheses. If a positive overflow occurs, 7FFFH is input; 8000H is input if a negative overflow occurs.

(e) Flag operation by ALU function

ALU function	FLAG			
	C	Z	OV	S
NOP	°	°	°	°
CLR	0	1	0	0
INC	↕	↕	↕	↕
DEC	↕	↕	↕	↕
CPL1	0	↕	0	↕
CPL2	0	↕	0	↕
SHRA	↕	↕	0	↕
SHLA	↕	↕	0	↕
SHR1	↕	↕	0	↕
SHL1	↕	↕	0	↕
SHR2	0	↕	0	↕
SHL2	0	↕	0	↕
SHR4	0	↕	0	↕
SHL4	0	↕	0	↕
SWAP	0	↕	0	↕

ALU function	FLAG			
	C	Z	OV	S
OR	0	↕	0	↕
AND	0	↕	0	↕
XOR	0	↕	0	↕
SUB	↕	↕	↕	↕
ADD	↕	↕	↕	↕
SBB	↕	↕	↕	↕
ADC	↕	↕	↕	↕
MIN	↕	↕	↕	↕
CMPR	↕	↕	↕	↕
SUBI	↕	↕	↕	↕
SUBP	↕	↕	↕	↕
ADDP	↕	↕	↕	↕
SBBP	↕	↕	↕	↕
ADCP	↕	↕	↕	↕

°: The previous status is held

↕: Affected by the result of the operation

0: Reset

(f) Registers specified by RS field

RS field				Specified register
D3	D2	D1	D0	
0	0	0	0	No register is specified.
0	-	-	-	(Inhibited)
1	0	0	0	GR 0
1	0	0	1	GR 1
1	0	1	0	GR 2
1	0	1	1	GR 3
1	1	0	0	GR 4
1	1	0	1	GR 5
1	1	1	0	GR 6
1	1	1	1	GR 7

(g) Function specified by GM field

GM field				Function	
D3	D2	D1	D0		
0	0	0	0	No operation	
0	0	0	1	Accesses RAMG lower byte	(ACCE)←2
0	0	1	0	Accesses RAMG higher byte	(ACCE)←1
0	0	1	1	Accesses RAMG word	(ACCE)←0
0	1	0	0	Resets SL	(SL)←0
0	1	0	1	Sets SL	(SL)←1
0	1	1	0	Sets bank 2	(SL)←1, (H)←0
0	1	1	1	Sets bank 3	(SL)←1, (H)←1
1	0	0	0	Resets IOB	(IOB)←0
1	0	0	1	Sets IOB	(IOB)←1
1	0	1	0	Resets INTR	(INTR)←0
1	0	1	1	Sets INTR	(INTR)←1
1	1	0	0	Resets DF	(DF)←0
1	1	0	1	(Disabled)	
1	1	1	0	Starts D	MSB of PC1←0
1	1	1	1	Stops D	MSB of PC1←1

(ACCE): The 8th and 9th bits of the GARG
(H) : The 7th bit of the GARG
(SL) : The 6th bit of the GARG
(IOB) : IOB flag

4.2 D-INSTRUCTION

All the instructions for D-PART (hereinafter referred to as "D-INSTRUCTION") consist of one machine instruction per word. The D-INSTRUCTIONs are classified into two types according to the contents of the most significant bit (MSB) as shown below.

D-INSTRUCTION Classification by DOP Code

D15	Operation instruction
0	DOP instruction
1	DLD instruction

(1) DOP instruction

The DOP instruction includes all the instructions except for the immediate data load instruction.

Field Configuration of DOP Instruction

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	DC				S		R			SUBOF		SUBIF		ADDF	

Each field is described below.

(a) DC field

This field specifies the functions to control D-PART and to interface D-PART with IO-PART or G-PART.

(b) S field

This field specifies the input register for the SUB1. The selected input register becomes valid from the next instruction.

(c) R field

This field specifies the data to be read from RAMA or RAMB and the control of the address counter. The value of the RCNT can be changed after the data has been read. The new value becomes valid from the next read instruction.

(d) SUB0F and SUB1F fields

These fields specify the function of subtracters SUB0 and SUB1.

(e) ADDF field

These fields specify the function of adders ADD0 or ADD1.

Functions Specified by DC Field

DC field				Function	
D14	D13	D12	D11	Mnemonic	Operation
0	0	0	0	NOP	No operation
0	0	0	1	-	Disabled
0	0	1	0	DLJ	Decrements $LCNT_L$ If not zero, jumps to (BAR_L)
0	0	1	1	DHJ	Decrements $LCNT_H$ If not zero, jumps to (BAR_H)
0	1	0	0	RDF	Resets DF
0	1	0	1	SDF	Sets DF
0	1	1	0	MA	DRG0←A1, DRG1←B1
0	1	1	1	MAS	DRG0←A1, DRG1←B1, Sets DF
1	0	0	0	ML0	DRG0←L0, DRG1←L1
1	0	0	1	ML0S	DRG0←L0, DRG1←L1, Sets DF
1	0	1	0	ML2	DRG0←L2, DRG1←L3
1	0	1	1	ML2S	DRG0←L2, DRG1←L3, Sets DF
1	1	0	0	RIOB	Resets IOB
1	1	0	1	SIOB	Sets IOB
1	1	1	0	WIOB	Waits until IOB="0"
1	1	1	1	WAIT	Waits

Registers Specified by S Field

S field		Mnemonic	Function	
D10	D9		P1 input	Q1 input
0	0	NOP	(Unchanged)	(Unchanged)
0	1	L0W2	L0	W2
1	0	A2B1	A2	B1
1	1	A2W2	A2	W1

Functions Specified by R Field

R field			Function	
D8	D7	D6	Mnemonic	Operation
0	0	0	NOR	No read
0	0	1	WB1	(WCNTA)$_H$: Add 1, (WCNTA)$_L$ ← 0 (WCNTB)$_H$: Add 1, (WCNTB)$_L$ ← 0
0	1	0	WB2	(WCNTA)$_H$: Add 1, (WCNTA)$_L$ ← 0 (WCNTB)$_H$: Add 2, (WCNTB)$_L$ ← 0
0	1	1	(Inhibited)	
1	0	0	R	Read only
1	0	1	RI	Read, (RCNT)$_L$: Add 1
1	1	0	RC1	Read, (RCNT)$_H$: Add 1, (RCNT)$_L$ ← 0
1	1	1	RC2	Read, (RCNT)$_H$: Add 2, (RCNT)$_L$ ← 0

Functions Specified by SUBOF Field

D5	D4	Mnemonic	Function
0	0	NOP	No operation
0	1	SUB	L0 ← P0 - Q0
1	0	SUBA	L0 ← Absolute (P0 - Q0)
1	1	SUBT	If $P0 \geq Q0$: L0 ← P0 - Q0 If $P0 \leq Q0$: L0 ← "0"

Functions Specified by SUB1 Field

D3	D2	Mnemonic	Function
0	0	NOP	No operation
0	1	SUB	L1 ← P1 - Q1
1	0	SUBA	L1 ← Absolute (P1 - Q1)
1	1	SUBT	If P1≥Q1: L1 ← P1 - Q1 If P1≥Q1: L1 ← "0"

Functions Specified by ADDF Field

D1	D0	Mnemonic	Function
0	0	NOP	No operation
0	1	-	Inhibited
1	0	ADD	L2 ← L2+P2, L3←L3+P3
1	1	MOV	L2 ← P2, L3←P3

(2) DLD instruction

This is an immediate data load instruction.

Field Configuration of DLD Instruction

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DOP	DEST			I M D											

The DLD instruction has the following functions.

° Outputs the contents of the IMD field to the register specified by the DEST field.

° Increments the PC1.

(a) DEST field

This field specifies the destination register to which data in the IMD field is to be transferred.

(b) IMD field

This field stores data that is to be transferred to the register specified by the DEST field. The data is transferred so that bit D0 is transferred to the least significant bit (LSB) of the specified register and rest of the bits are discarded.

Registers Specified by DEST Field

DEST field			Mnemonic	Register
D14	D13	D12		
0	0	0	RCNT	RCNT
0	0	1	PC1	PC1
0	1	0	LCNT$_L$	LCNT$_L$ (Lower 8 bits)
0	1	1	LCNT$_H$	LCNT$_H$ (Higher 8 bits)
1	0	0	BAR$_L$	BAR$_L$ (Lower 6 bits)
1	0	1	BAR$_H$	BAR$_H$ (Higher 6 bits)
1	1	0	WCNTA	WCNTA
1	1	1	WCNTB	WCNTB

4.3 IO-INSTRUCTION

The instructions for IO-PART (IO-INSTRUCTIONs) are stored in IOSR1 and IOSR2.

Field Configuration of IOSR1 and IOSR2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT								PBUS SRC		PBUS DST		RC	SL	WS	

The IO-INSTRUCTION has the following functions.

(a) When the IOB flag is "0", no operation is performed.

(b) The operations described in (c) and (d) below are performed first to IOSR1 and then to IOSR2.

(c) Repeats the operation described in (d) below the number of times specified by the COUNT field.

(d) Inputs the contents of the register specified by the PBUS SRC to the register specified by the PBUS DST via the PBUS.

(e) Resets the IOB flag.

Each field is described below.

(a) COUNT

This field indicates the number of times by which the input/output operation is to be performed.

(b) PBUS SRC

This field specifies the register that is to output data to the PBUS.

(c) PBUS DST

This field specifies the register that is to input data from the PBUS.

(d) RC

This field specifies the number of bits to be transferred at a time.

(e) SL

This field specifies RAMA or RAMB.

(f) WS

This field specifies the method by which data is written from the DBUF to RAMA or RAMB.

Registers Specified by PBUS SRC Field

D7	D6	Specified register
0	0	DR
0	1	IR
1	0	PDBUF
1	1	A1

Registered specified by PBUS DST Field

D5	D4	Specified register
0	0	DR
0	1	IR
1	0	PDBUF
1	1	DBUF

Function Specified by RC Field

D3	No. of bits to be transferred
0	8
1	16

Function Specified by SL Field

D2	Data write RAM	RAMA/RAMB address register	External RAM address register
0	RAMA	WCNTA	PCNTA
1	RAMB	WCNTB	PCNTA

Function Specied by WS Field

D1	D0	Method to write data from DBUF to RAMA or RAMB
0	0	8 bits of DBUF are written to RAMA or RAMB.*
0	1	Lower 4 bits of DBUF are written to RAMA or RAMB.*
1	0	Higher 4 bits and then lower 4 bits of DBUF are written to the corresponding lower bits** of RAMA or RAMB.*
1	1	Inhibited

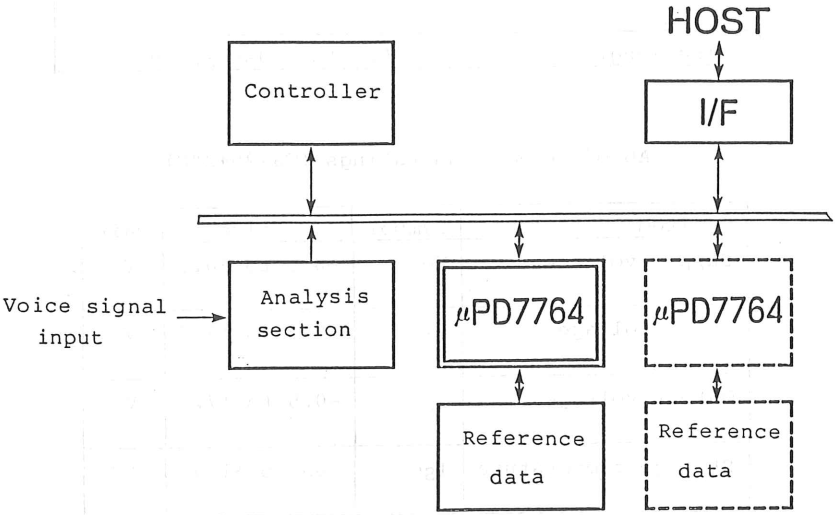
* The SL field is used to specify RAMA or RAMB.

** Two 4-bit data are written to lower nibbles of the adjacent 2 bytes of the specified RAM and the higher nibbles of the 2 bytes all become 0.

4.4 Basic Utilities Stored in ROM

Start address	Module ID	Function	Ref. Reg.	Mod. Reg.
80H	INIT	Program loading	SR MC PC1	MC=0H PC1=20H PC2=0H IM1, IM2 GR7
92H	RST2	G program loading		SR=0H MC=0H PC2=0H IM2, GR7
A0H	LMIM 2	Data is written from external device to externally specified address of IM2	SR	MC IM2 (MC)
A3H	LIM 2	Data is written from external device to internally specified address of IM2	SR MC	MC=+1H IM2 (MC)
DEH	UINA 1	Inputs 2 bytes of pattern memory to IR	PCNTA	PCNTA=+2H IOSR1=0H IOSR2=0H IR
EGH	UINB 1	Inputs 1 byte of pattern memory to IR	PCNTA	PCNT=+1H IOSR1=0H IOSR2=0H IR
E9H	MULTI	Multiplication	GR0 GR1	GR0, GR1 GR2 GR3=0H
F2H	DIVID	Division	GR0 GR1	GR0, GR1 GR2 GR3=0H GR4

Note: Ref. Reg.: Register referenced within a module
Mod. Reg.: Register whose value changes within a module



System Configuration of High-Performance
Voice Recognition LSI

Performance Example of Voice Recognition

Item	Example 1	Example 2
Recognition classification	Connected-word	Isolated-words
No. of words	40 words max. per chip	340 words max. (128K bytes)
Recognition algorithm	2-level DP matching	DP matching
Host CPU (example)	µPD8086	µPD8085
Response time	0.3sec max.	
Recognition accuracy	99% max.	
Voice length	0.2 to 4.0sec/word	

Absolute Maximum Ratings (Ta=25±2°C)

Item	Symbol	Value	Unit
Supply voltage	V_{CC}	-0.5 to +0.7	V
Input voltage	V_I	-0.5 to +7.0	V
Output voltage	V_O	-0.5 to +7.0	V
Storage temperature	T_{STG}	-65 to +150	°C

Recommended Operating Conditions

(1) DC conditions

(Ta=-10 to +70°C, V_{CC}=+5V±10%)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}		4.5		5.5	V
Input voltage	V_I		-0.5		V_{CC}+0.5	V
Low level input voltage	V_{IL}	Excluding CLK	-0.5		0.8	V
	V_{IL1}	CLK	-0.5		0.45	V
High level input voltage	V_{IH}	Excluding CLK	2.0		V_{CC}+0.5	V
	V_{IH1}	CLK	3.9		V_{CC}+0.5	V

(2) AC conditions

(Ta=-10 to +70°C, V_{CC}=+5V±10%)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
CLK cycle time	t_{CY}		125		500	ns
CLK low level width	t_{CL}		50			ns
CLK high level width	t_{CH}		55			ns
CLK rise time	t_r				10	ns
CLK fall time	t_f				10	ns
Set up time of A_0, C_S, $\overline{\text{DACK}}$ (to $\overline{\text{RD}}$)	t_{AR}		0			ns
Hold time of A_0, C_S, $\overline{\text{DACK}}$ (from $\overline{\text{RD}}$)	t_{RA}		0			ns
RD pulse width	t_{RR}		200			ns
Set up time of A_0, C_S, $\overline{\text{DACK}}$ (to $\overline{\text{WR}}$)	t_{AW}		0			ns
Hold time of A_0, C_S, $\overline{\text{DACK}}$ (from $\overline{\text{WR}}$)	t_{WA}		0			ns
WR pulse width	t_{WW}		150			ns
Data set up time (to $\overline{\text{WR}}$)	DW		100			ns
Data hold time (from $\overline{\text{WR}}$)	t_{WD}		0			ns
Memory data input set up time to $\overline{\text{WR}}$	t_{DSC}		80			ns
Memory data input hold time from $\overline{\text{WR}}$	t_{DHC}		0			ns
$\overline{\text{DACK}}$ delay time	t_{DACK}		0			ns

Electrical Characteristics

(1) DC characteristics

(Ta=-10 to +70°C, V_{CC}=+5V±10%)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Low level output voltage	V_{OL}	I_{OL}=2.0mA			0.45	V
High level output voltage	V_{OH}	I_{OH}=-400μA	2.4			V
Low level input leakage current	I_{LIL}	V_{IN}=0V			-10	μA
High level input leakage current	I_{LIH}	V_{IN}=V_{CC}			10	μA
Low level output leakage current	I_{LOL}	V_{OUT}=0.45V			-10	μA
High level output leakage current	I_{LOH}	V_{OUT}=V_{CC}			10	μA
Supply voltage	I_{CC}				280	mA

(2) Capacity

(Ta=25, V_{CC}=0V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
CLK capacity	C_{ϕ}				20	pF
Input capacity	C_{IN}	f_C=1MHz			10	pF
Output capacity	C_{OUT}				20	pF

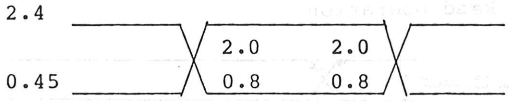
(3) AC characteristics (Ta=-10 to +70°C, V_{CC}=+5V±10%)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Data access time (from $\overline{\text{RD}}$)	t_{RD}	C_L=100pF			150	ns
Data floating time (from $\overline{\text{RD}}$)	t_{DF}	C_L=20pF, RL=2kΩ	0		100	ns
DRQ delay time	t_{AM}				150	ns
$\overline{\text{RAS}}$ precharge time	t_{RP}		180			ns
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t_{RCD}		190	190	310	ns
$\overline{\text{RAS}}$ hold time	t_{RSH}		190	190		ns
Row address set up time to $\overline{\text{RAS}}$	t_{ASR}		40	125		ns
Row address hold time from $\overline{\text{RAS}}$	t_{RAH}		65	125		ns
Column address set up time to $\overline{\text{CAS}}$	t_{ASC}		45	125		ns
Column address hold time from $\overline{\text{CAS}}$	t_{CAH}		250	375		ns
$\overline{\text{CAS}}$ pulse width	t_{CAS}		190	250	310	ns
Data output set up time to $\overline{\text{CAS}}$	t_{DS}		300	375	500	ns
Data output hold time from $\overline{\text{CAS}}$	t_{DH}		150	250	320	ns
$\overline{\text{WE}}$ set up time to $\overline{\text{CAS}}$	t_{WCS}		50	125		ns
$\overline{\text{WE}}$ hold time from $\overline{\text{CAS}}$	t_{WCH}		150	250		ns
Memory cycle time	t_{RC}		690	750		ns
Refresh period	t_{REF}		512		576	μs

Note: 1. Voltage of AC timing measuring point

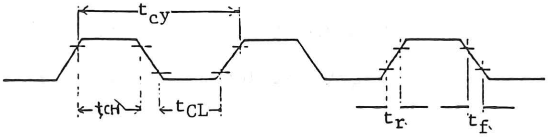
° Excluding CLK	° CLK
$V_{IL}=V_{OL}=0.8V$	$V_L=0.45V$
$V_{IH}=V_{OH}=2.0V$	$V_H=3.9V$

2. Input waveform of AC test (Excluding CLK)

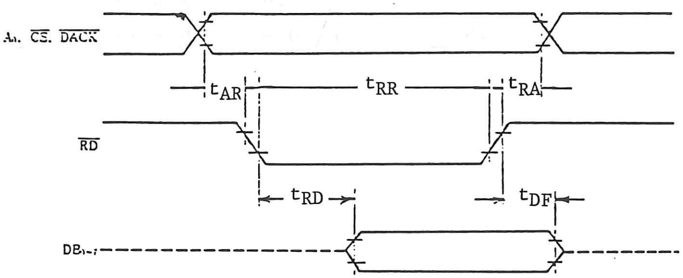


Timing Diagram

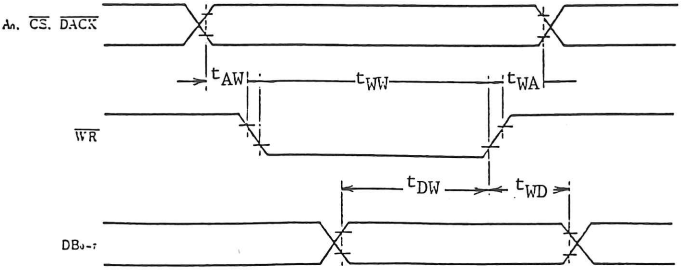
Clock



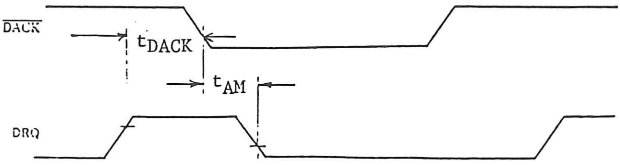
Read operation



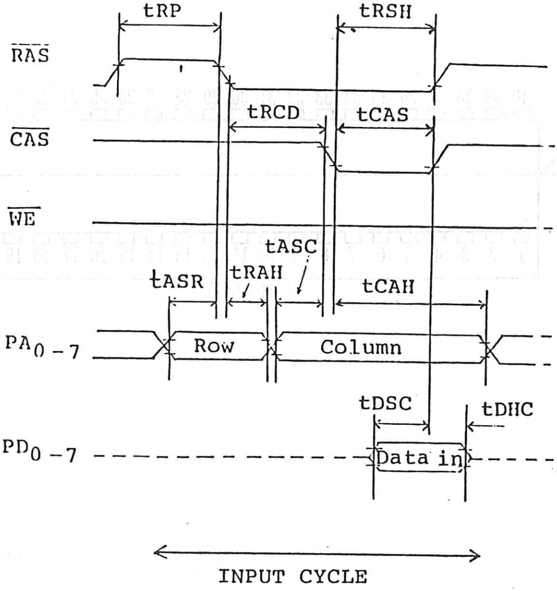
Write operation

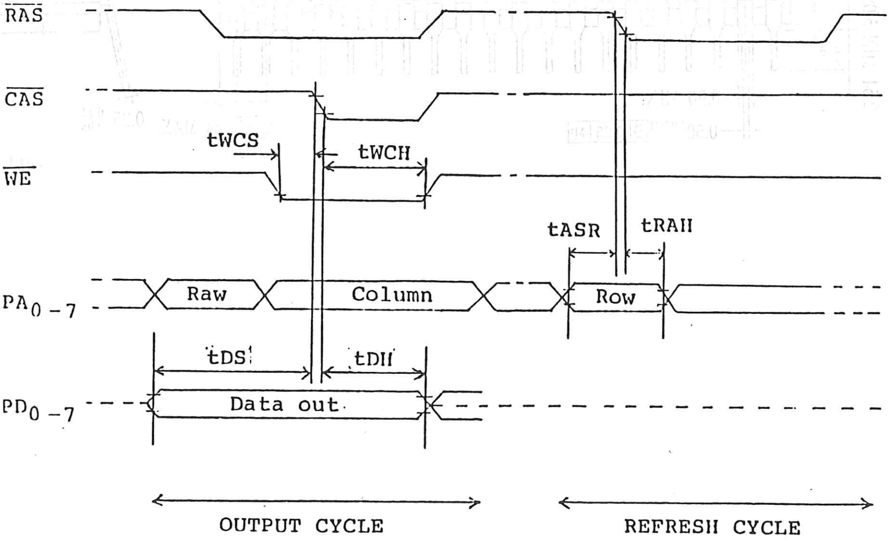


DMA operation

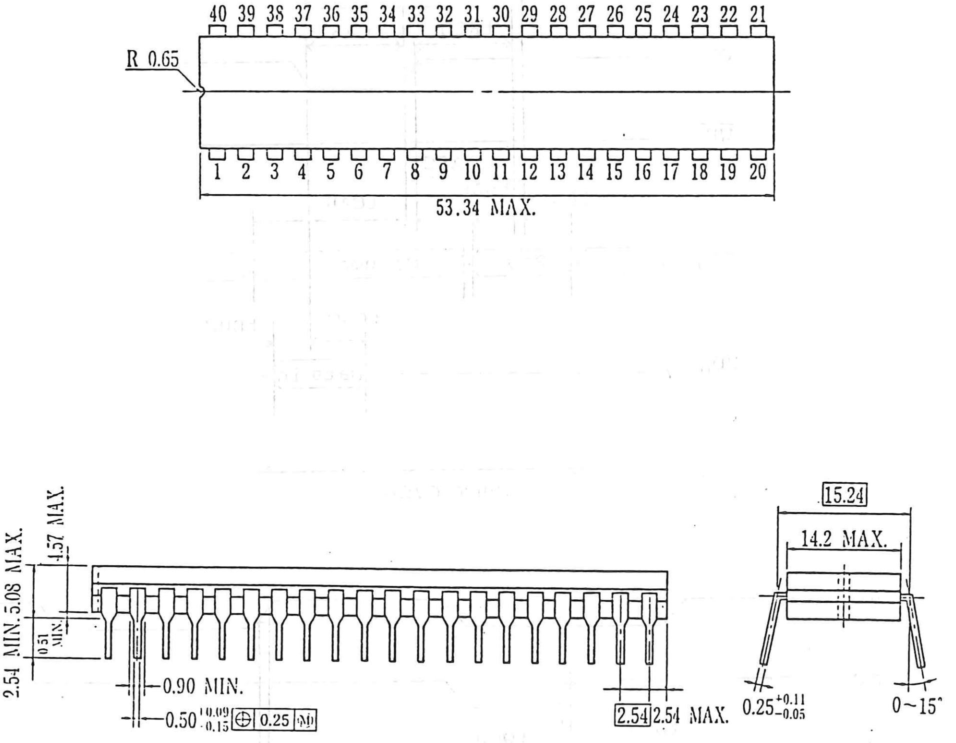


Memory Input/Output Timing





Outline Dimensioned Drawing of 40-Pin Ceramic DIP (Unit: mm)



40DH-100-600

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